THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 14

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Appeal No. 1997-3730 Application No. 08/095,147

ON BRIEF

Before JERRY SMITH, KRASS, and RUGGIERO, <u>Administrative Patent</u> <u>Judges</u>.

RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal from the final rejection of claims 1 to 14, all of the claims pending in the present application. Claims 15 to 20 have been canceled. An

amendment after final rejection filed April 10, 1995, was denied entry by the Examiner.¹

The claimed invention relates to a device for reducing plasma etch damage occurring within a sputter etch chamber as a result of undesirable charge transfer or arcing between the chamber anode and a semiconductor wafer surface. More particularly, a diode which acts to prevent undesirable charge transfer is formed within an inactive region of the wafer in registry with the wafer coupling retainer. In a further embodiment, instead of being placed on the wafer, a charge transfer prevention diode is placed between the sputter etch anode plate and a ground terminal.

Claim 1 is illustrative of the invention and reads as follows:

1. A device for reducing plasma etch damage occurring within a sputter etch chamber, comprising:

¹ The amendment after final rejection proposed entry of new claims 21 to 25. In an Advisory Action mailed April 20, 1995, the Examiner indicted substantive reasons for denying entry of the amendment although the box in item 3 on Form PTOL 303 indicating entry of the amendment was apparently inadvertently checked. Appellants' May 12, 1995, response to the Advisory Action verifies Appellants' understanding that the amendment after final was not to be entered and that only claims 1 to 14 are the subject of this appeal.

an anode spaced from a retainer of a sputter etch chamber;

said retainer retaining a semiconductor wafer having an inactive region and an active region;

at least one diode formed within said inactive region of said wafer near the outer periphery of said wafer; and

said diode is capable of electrical connection to said retainer.

The Examiner relies on the following prior art:

Dean et al. (Dean) 1984	4,473,455	Sep.	25,
Tai et al. (Tai)	4,496,448	Jan.	29,
Harrington, III (Harrington) 24, 1990	4,943,537		Jul.
Lee et al. (Lee) 1994	5,292,399	Mar.	08,
	(Filed Jan.	08,	1992)

Singer, Peter H., "Evaluating Plasma Etch Damage," <u>Semiconductor International</u>, pp. 78-81 (May 1992).

Claims 1 to 14 stand finally rejected under 35 U.S.C. §

103. As evidence of obviousness, the Examiner offers Singer
in view of Harrington and Lee with respect to claims 1 to 5,

adding Dean to the basic combination with respect to claim 6,

and adding Tai to the basic combination with respect to claims

7 to 14.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Brief and Answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the Examiner and the evidence of obviousness relied upon by the Examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellants' arguments set forth in the Brief along with the Examiner's rationale in support of the rejection and arguments in rebuttal set forth in the Examiner's Answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claims 1 to 14. Accordingly, we reverse.

In rejecting claims under 35 U.S.C. § 103, it is

incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. See <u>In re Fine</u>, 837

F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the Examiner is expected to make the factual determinations set forth in <u>Graham v. John Deere Co.</u>, 383 U.S. 1,

17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to

modify the prior art or to combine prior art references to arrive

at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole

or knowledge generally available to one having ordinary skill in

the art. <u>Uniroyal Inc. v. Rudkin-Wiley Corp.</u>, 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), <u>cert. denied</u>, 488 U.S. 825

(1988); Ashland Oil, Inc. v. Delta Resins & Refractories,
Inc.,

776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert.

denied, 475 U.S. 1017 (1986); ACS Hosp. Sys., Inc. v.

Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the Examiner are an essential part

of complying with the burden of presenting a <u>prima facie</u> case of

obviousness. Note <u>In re Oetiker</u>, 977 F.2d 1443, 1445, 24 USPQ2d

1443, 1444 (Fed. Cir. 1992).

With respect to the Examiner's obviousness rejection of independent claims 1 and 7, Appellants assert (Brief, page 19) that the Examiner has failed to establish a <u>prima facie</u> case of obviousness since none of the references suggest any reason why they might be combined. Further, Appellants assert that, even if the references could be combined, the resulting combination would not meet the requirements of the claimed invention.

After careful review of the applied prior art in light of the arguments of record, we are in agreement with Appellants' position as stated in the Brief. We note that a relevant portion of independent claim 1 recites:²

at least one diode formed within said inactive region of said wafer in registry with said retainer and near the outer periphery of said wafer; ...

In addressing this limitation, the Examiner initially calls attention to Lee which is directed to the prevention of arcing in plasma etch systems. As correctly set forth by the Examiner, Lee's approach to this problem is to provide a conductive path for electrical charges by inserting conductive plugs through the protective surfaces surrounding the wafer on the top surface of a metal pedestal. As motivation for incorporating the conductive plugs within an inactive region of a wafer as recited in the claims on appeal, the Examiner turns to the CMOS integrated circuit disclosure of Harrington. As asserted by the Examiner, the Figure 6 illustration and accompanying description in Harrington disclose the

² Independent claim 7, which is directed to the same embodiment of the invention, has a similar recitation.

establishment of diode depletion regions which act as a barrier to inhibit current flow through the buried channel region beneath a P-channel gate. In the Examiner's view, the skilled artisan, noting that the conductive plugs of Lee and the depletion regions of Harrington are made of the same material, would have been motivated to incorporate Lee's conductive plugs within the outer periphery of the inactive region of a wafer, such as illustrated in Singer, in view of Harrington's teachings of incorporating diodes on the surface of a semiconductor wafer.³

It is our view, however, that the charge transfer control techniques of Lee and Harrington are so opposite in approach that any motivation to combine them must have resulted from an improper attempt to reconstruct Appellants' invention in hindsight. As discussed previously, Lee's solution to the arcing problem in plasma etch systems is to provide a conductive path in the form of plugs to carry charge away from the wafer. On the other hand, Harrington, rather than

³ The Singer reference is relied upon by the Examiner as disclosing the presence of inactive regions on a semiconductor wafer surface.

providing an avenue for charge flow, erects a barrier to the flow of charge through buried channel regions of a semiconductor. In view of the above, we are left to speculate why one of ordinary skill would have found it obvious to modify the applied prior art to make the combination suggested by the Examiner. The only reason we can discern is improper hindsight reconstruction of Appellants' claimed invention. In order for us to sustain the Examiner's rejection under 35 U.S.C. § 103, we would need to resort to speculation or unfounded assumptions or rationales to supply deficiencies in the factual basis of the rejection before us. In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968), rehearing denied, 390 U.S. 1000 (1968).

We are further of the opinion that, as asserted by Appellants, even assuming <u>arguendo</u> that proper motivation were established for the Examiner's proposed combination, the resulting system would fall far short of meeting the specific requirements of the claims on appeal. The appealed claims set forth a specific positional relationship between the formed diode, the inactive region of the wafer, and the wafer

retainer. The Examiner has provided no indication as to how and where the skilled artisan might have found it obvious to modify the teachings of Singer, Lee, and Harrington to arrive at the claimed invention. The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 972 F.2d 1260,

1266, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992).

With respect to the Tai and Dean references, we note that these references were applied by the Examiner as disclosing the rf power and retainer clip features, respectively, of the appealed claims. We find no disclosure in either of these references that would overcome the innate deficiencies of Singer, Lee, and Harrington discussed <u>supra</u>. Accordingly, since the Examiner has not established a <u>prima facie</u> case of obviousness, the rejection of independent claims 1 and 7, and claims 2 to 6 and 8 to 12 dependent thereon, is not sustained.

We now turn to a discussion of independent claim 13 which is directed to the embodiment in which the claimed diode is placed between a ground terminal and the anode, rather than

within the inactive region of a wafer. In addressing the claim limitations, the Examiner proposes the same rationale and combination of references as set forth with regard to independent claims 1 and 7. In our view, the Examiner's obviousness rejection of independent claim 13 can not be sustained for all of the reasons discussed supra. We do note that, as pointed out by the Examiner at page 9 of the Answer, the drawing in Figure 2 of Tai illustrates a diode placed between the anode and ground in a plasma etch system. Although this disclosure of Tai would appear to read directly on a key feature of Appellants' independent claim 13, this claimed feature cannot be considered in isolation. Our review of claim 13 reveals that the charge transfer prevention diode is recited in combination with several other features of the etch damage prevention device including a specific positional relationship between the anode, cathode, wafer, and the specific wafer retainer structure. In our view, for all of the reasons discussed supra, any proposed combination of the applied prior art that could result in the claimed invention must be an exercise in improper hindsight reconstruction. From our earlier discussion, we remain convinced that the

solutions of Lee and Harrington to the undesirable charge transfer or arcing problem are completely opposite in approach. Further, the problem of excess electrode DC bias addressed by the Zener diode placement in Tai does not appear to exist in Lee, Harrington, or any of the other prior art of record. Accordingly, the Examiner's obviousness rejection of independent claim 13, and of claim 14 dependent thereon cannot be sustained.

In summary, we have not sustained the Examiner's 35 U.S.C.

§ 103 rejection of any of the claims on appeal. Thus, the Examiner's decision rejecting claims 1 to 14 is reversed.

REVERSED

JERRY SMITH)			
Administrative	Patent	Judge)			
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)	BOARD	OF	PATENT

ERROL A. KRASS) APPEALS

Administrative Patent Judge) AND
) INTERFERENCES
)
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Leticia

Appeal No. 1997-3730 Application No. 08/095,147

APJ RUGGIERO

APJ KRASS

APJ JERRY SMITH

DECISION: REVERSED

Send Reference(s): Yes No

or Translation (s)
Panel Change: Yes No

Index Sheet-2901 Rejection(s):

Prepared: March 22, 2001

Draft Final

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OB/HD GAU

PALM / ACTS 2 / BOOK DISK (FOIA) / REPORT